Solid State TECHNOLOGY
THE INTERNATIONAL MAGAZINE FOR SEMICONDUCTOR MANUFACTURING

## WAFER CLEANING

# Why wafer cleaning becomes more challenging

In the 2004 update of the ITRS, many targeted milestones for wafer cleaning remain unchanged from the previous year, but near-term and long-term requirements will undergo greater scrutiny during the drafting of the 2005 ITRS.

Requirements for front-end-of-line (FEOL) surface preparation are being driven by both device scaling and new materials introduction. Device scaling is closing the process window in which cleaning efficiency is balanced with surface etching and pattern damage. Removal of particle contaminants requires either chemical reaction (bond-breaking) or physical force to overcome adhesion forces. The challenge is to supply enough chemical reaction or physical force to remove contaminants without removing excessive Si from the source and drain or $SiO_2$ from the isolation trench, without adding excessive surface roughness, and without damaging patterned features such as the narrow gate electrode.

In the interconnect segment, stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of low-*k* films in the insulating layers. Current etch and strip methods can damage new porous low-*k* films by removal of the carbon species. After subsequent wet cleans, critical dimension changes may be significant. Many dry methods of cleaning as well as new rinsing and drying techniques require more work (see Fig. 2 on p. 30).

In FEOL surface preparation, many different approaches are under investigation to meet this challenge, including improvements to traditional batch wet-cleaning approaches, development of new single-wafer wet-cleaning approaches, application of gaseous aerosol approaches, and the use of supercritical fluids. Solutions appear to be identified for the 65nm technology node, but it is not clear yet whether current approaches can meet the 45nm technology node material-loss restrictions and still achieve sufficient cleaning efficiency to meet defectivity requirements.

The introduction of high-*k* materials has presented a challenge to surface preparation both in predeposition cleaning and in the need to remove high-*k* dielectric films from source and drain regions after formation of the gate electrode. High-*k* gate dielectric material is deposited on top of the silicon surface, whereas silicon oxide gate dielectric is formed by oxidizing the silicon surface. Because the high-*k* material is deposited, predeposition cleaning and surface preparation must be carefully controlled. Standard cleaning processes can easily leave a surface either oxide-free or with a 10Å layer of oxide. Ideally, one would like a very thin oxide layer of 2–5Å on the surface before high-*k* deposition. Processes to meet this challenge are under development. The removal of high-*k* material after gate electrode formation must be carried out with high selectivity to the gate electrode, to the isolation dielectric, and to the underlying silicon. Standard cleaning processes are not able to achieve the required selectivity. It appears that a combination of dry and wet processes will be required to meet the needs of this selective removal process and are under development. ■

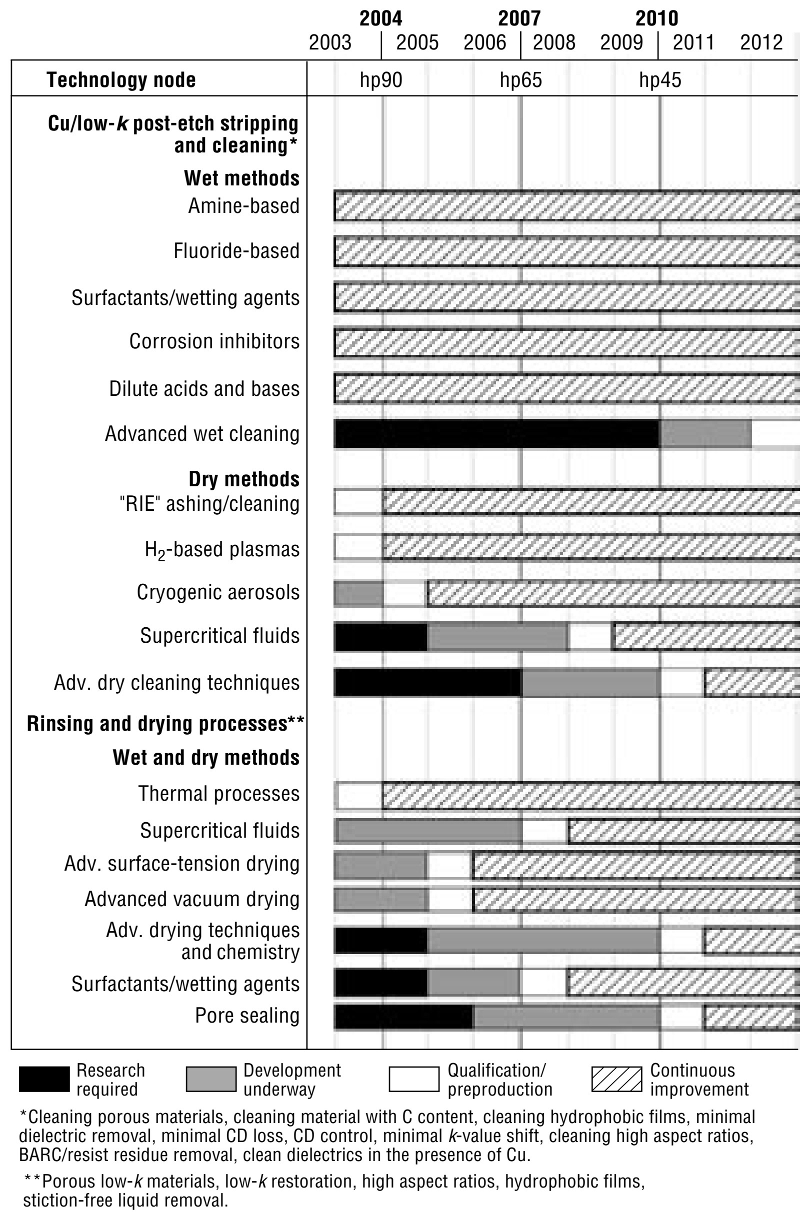


**Figure 2.** Potential solutions for interconnect surface preparation.

*Jeffery W. Butterbaugh* is co-chair of the ITRS Frontend Processing working group and chief technologist at FSI International.

**Jeffery W. Butterbaugh,** FSI International Inc., Chaska, Minnesota
**Christopher Case,** BOC Edwards, Murray Hill, New Jersey